REMARKS

Claims 1 - 4 remain active in this application. Amendment of claims 1 - 4 has been requested to more affirmatively recite elements thereof, to eliminate unnecessary reference to a specific standard and to make changes in claim 1 to correspond to amendments previously made in claim 3. Support for the amendments of the claims is found throughout the application, particularly in Figures 4, 5 and 6 and the description thereof on pages 3 - 5 and 12 - 14. Accordingly, no new issue can be raised by such amendment containing recitations present in another claim as finally rejected. No new matter has been introduced into the application.

Claims 1 - 2 have again been rejected under 35 U.S.C. §103 as being unpatentable over Kawahara et al. in view of the SGS-Thompson publication and claims 3 - 4 have again been rejected under 35 U.S.C. §103 as being unpatentable over Kawahara et al. in view of the SGS-Thompson publication and the further teachings of Kobayashi et al. These grounds of rejection are respectfully traversed for the reason set forth in the previous response, which is hereby fully incorporated by reference, and the further remarks provided below.

The Examiner's attention is respectfully called to pages 6 - 8 of the previous response filed February 20, 2004, for a detailed description of the invention in comparison with the prior art under the IEEE 1394 standard. In summary, as shown in Figures 2 and 3 and discussed on pages 3 - 8 of the present application, nodes connected to a bus can be powered either from the bus or by its own internal power supply. Power requirements of the respective nodes connected to the bus and power provided to them over the bus are managed by a bus manager which collects power class information from the respective nodes as the nodes initially

receive power and are disconnected from and reconnected to the bus responsive to the output of the power-on reset circuit.

As pointed out in the paragraph bridging pages 6 and 7 of the present specification and discussed in detail in the remarks appended to the previous response, the power-on reset circuit causes reset of the physical layer, PHY, and the bus and generation of self-identification information including power class information to be provided to the bus manager node for management of the power distribution to the other nodes connected to the bus only when power is initially applied to the node (e.g. after some period when no power is applied to the node either from the bus or the internal power supply of the node).

In a conventional IEEE 1394 compliant node configured as illustrated in "Prior Art" Figure 2 or 3, the power-on reset circuit is responsive to the output of a DC-DC converter 4 which, in turn, receives power from either of two parallel-connected circuits: the internal power supply circuit 2 or the power terminals of the bus 9_1 and/or 10_1. Therefore, the physical layer, PHY, is prevented from distinguishing the source of the power for the node and, since the power connections to the DC-DC converter are in parallel and power would be supplied from the bus if power is not supplied from internal power supply 2 (or the power input thereto), the power-on reset circuit would not see any power interruption and restoration or initiation of supply of power from internal power supply 2 after the node is supplied with power from the bus and thus would not cause reset of PHY and the bus to generate new information in regard to a change of operating state of the internal power supply 2 while the data previously transmitted to the bus manager node remains unchanged and incorrect.

In essence, the invention avoids such a problem by

the simple expedient of adding a changing point detection arrangement to monitor the internal power supply of the node and to provide a signal path in parallel to the power-on reset circuit for causing reset when the operating state of the internal power supply changes. Both of these parallel arrangements for causing reset and the responsiveness of the physical layer circuit to *either* the power-on reset circuit *or* the changing point detection means are explicitly recited in *both* independent claims 1 and 3.

In contrast, as pointed out in the previous response:

> "Kawahara et al. teaches a device which monitors the local power supply and generates one of two codes (one indicating that power is not available from the local power supply and the other indicating the amount of power available) depending on the voltage available from the local power supply and provided as flag 26. This code is applied to the physical layer interface circuit (see column 6, lines 43 - 45) but Kawahara et al. is silent as to causing reset of the physical layer circuit or including transmission of the code to the bus manager upon change of power supply status after power application to PHY."

That is, Kawahara et al. does not appear to teach or suggest *either* a power-on reset circuit *or* a changing point detection means or any other arrangement to cause reset even upon initial application of power (essentially admitted by the Examiner in the rejection of claims 3 and 4 and citing Kobayashi et al. for its teaching of a power-on reset circuit) but only provides switching of power connections *within the node* in response to the state of the internal power supply of the node. In particular, there is no teaching or suggestion concerning reset of PHY in Kawahara. Even if reference is made to SGS-Thomson, only a power-on reset, but not a changing point detector (much less reset of PHY in response thereto), is disclosed.

Therefore, when the power supply supplied to PHY changes from bus power to self-power or vice-versa, reset of PHY is not performed and the power class supplied to PHY is not transmitted to a bus through a self-ID packet. Accordingly, the problem that the power supply currently supplied to PHY and the power class information previously outputted are different. Accordingly, the combination of Kawahara et al. and SGS-Thomson does not teach or suggest the combination of elements claimed or provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness since the combined teachings and suggestions thereof do not lead to an expectation of success in deriving the meritorious function of the invention.

The Examiner's statement of the rejection does not address these deficiencies in the teachings and suggestions of Kawahara et al. On the contrary, from the statement of the rejections, the Examiner not only seems to *assume* a power-on reset circuit in Kawahara et al. (which, in any event, is admitted to be prior art although the statements of the rejections do not appear to place any reliance thereon) but seems to confuse and equate the power-on reset circuit with the changing point detection means which, in accordance with the invention, as claimed, also causes reset of PHY and the bus even though no reset function *at all* appears to be taught or suggested by Kawahara et al. In summary, Kawahara et al. (since it develops a code) appears to be somewhat similar to the admitted prior art of Figure 3 but without inclusion of power-on reset circuit 11 and the distinction of the invention therefrom can be readily visualized by comparison with Figure 4 (or Figure 7, additionally illustrating the bus voltage detection unit 12 recited in dependent claims 2 and 4) of the present application which additionally includes a changing point detection means 8 having an output

connected to the same terminal of the PHY as the power-on reset circuit 11 in order to initiate reset upon change of internal power supply status *in addition to the reset function initiated by the power-on reset circuit* 11.

Thus, the deficiency of Kawahara et al. is not mitigated by the SGS-Thomson reference. While the SGS-Thomson reference includes a power-on reset function as discussed in detail in section 2.6 (pages 10 - 11) the initiation of the reset function is explicitly limited to power reset. This limitation is also essentially reiterated in section 2.8.7 (page 21) in which the status transfer is noted to be "initiated by the link in response to a register read request from the link device, or to indicate the nodes new phy_ID *after a bus reset...*" (emphasis added). In other words, the SGS-Thomson reference closely corresponds to the description of the prior art in the present application and does not include a changing point detection means for causing reset *in addition to the power-on reset circuit.* Therefore, the combination of Kawahara et al. and SGS-Thomson does not teach or suggest the subject matter of the invention beyond the admitted prior art and does not recognize the problem addressed by the changing point detection circuit and thus cannot lead to an expectation of success in overcoming the problem or otherwise provide evidence of a level of ordinary skill in the art which would support the *conclusion* of obviousness which the Examiner has asserted. By the same token, by confusing the reset function responsive to the changing point detection means with the power-on reset function of the admitted prior art or SGS-Thomson (upon which the Examiner does not appear to rely) the Examiner has failed to make a *prima facie* demonstration of obviousness of any claim in the application.

In regard to the Examiner's apparent confusion regarding the reset of PHY and the bus reset in

response to configuration change, the Examiner may not understand the mechanism to which the power class information is output causing the Examiner's position to be inapposite and contradictory. Accordingly, the following explanation is provided to assist the Examiner's appreciation of the distinctive features of the invention.

Almost all PHYs include a PHY substantially as described in the SGS-Thomson reference based on the IEEE 1394 standard. By performing power-on reset,, these PHYs change to a bus reset sequence mode and establish a bus through a Tee-ID sequence and a Self-ID sequence. The power class code supplied to PHY is embedded in the Self-ID packet generated in a Self-ID sequence and is output to a bus. When the self-power supply is supplied to PHY, the power class information that indicates operation by the self-power supply is output to the bus and when the bus power supply is supplied to PHY, the power class information which indicates operation by the bus power supply is out put to the bus. However, when the power class information is changed after the power supply is switched on, power-on reset is not generated since the power supply voltage does not change. Consequently, a Self-ID packet is not generated and the changed power class information is not output to the bus. In other words, the power supply supplied to a node changes after the power supply is supplied to PHY (for example, from a bus power supply to a self-power supply of vice-versa), the power class code supplied to PHY changes but the changed power class code is not output to the bus because a Self-ID packet is not output to the bus. In order to output the changed power class code to the bus, it is necessary to reset PHY and to output a Self-ID packet to the bus after the power class code is supplied to PHY.

If PHY is not reset, the changed power class code

is output to the bus only when the PHY detects a change in connection configuration of the bus. Therefore, the state that the power class information output to the bus and the power supply currently supplied to the node may differ and will be contradictory during the period after the power supply to a node changes until the PHY detects a change of connection configuration.

The operation of resetting the bus by connection configuration change is set by the IEEE 1394 standard. In this operation, when a power supply of the node is connected to the bus is switched on or the composition of a bus changes such as by the addition to or removal from the bus of a node (e.g. changing the number of nodes connected to the bus), PHY will detect the change of connection configuration and perform a bus reset sequence, a Tree-ID sequence and a Self-ID sequence to reconstruct the bus. The bus power supply or the self-power supply is supplied to PHY when neither power supply has been supplied to PHY immediately before and this condition is thus well-described by the phrase "a power supply of the node connected to the bus is switched on". In this case, since a new node is added to the bus or a node is removed from the bus, the connection configuration of the bus changes and, consequently, the bus reset occurs and the sequence of bus reconstruction is started. However, when the bus power supply is supplied to PHY, and the power supply supplied to PHY changes, from a bus power supply to a self-power supply, the supplied voltage (*at* PHY) does not change (unless, of course, the voltage is turned off) and thus power-on reset does not occur and the number of nodes connected to the bus will not be changed and the connection configuration will not be changed.

Therefore, while power is being supplied to PHY and the power supply is changed between the bus power supply and the self-power supply, PHY cannot detect the

change of connection configuration. Thus, the power supplied to PHY and the power class information previously output become different.

In summary, even if detection of a change of connection configuration is performed as in the conventional power-on reset and specified in the IEEE 1394 standard, changed of the power supply without a change in number of nodes connected to the bus or power interruption cannot be detected. Therefore, while power is being supplied to PHY and the power supply to PHY is changed between the bus power supply and the self-power supply, a change of power class information cannot be output to the bus.

In contrast, in accordance with the present invention, the changing point detector detects the change of voltage *at the self-power supply* (rather than at PHY where no voltage change is detectable), resets PHY and separates it from the bus. Then, a bus reset is generated and a Self-ID packet is generated including the changed power class code and output to the bus. Consequently, the power supply currently supplied to the node and the power class information for the node will be in agreement.

Thus, it is clearly seen that the teachings, suggestions and/or evidence of the level of ordinary skill in the art provided by Kawahara et al. and SGS-Thomson are insufficient to support a conclusion of obviousness which the Examiner has asserted. The deficiencies of Kawahara et al. and SGS-Thomson to answer the recitations of the claims are not mitigated by Kobayashi. In Kobayashi, when the connection configuration of a bus changes, PHY detects the change and generates a bus reset. That is, Kobayashi discloses performing a bus reset only when the connection configuration of a bus changes In Kobayashi, since the reset of PHY is not performed even if the power supply to/in a node changes, the state of

the node and the state of the bus do not change. Therefore, Kobayashi does not avoid an occurrence of a difference between the power supply being supplied to a node and the power class information previously output. Therefore, the teachings, suggestions and/or evidence of the level of ordinary skill in the art supplied by Kobayashi do not supplement those of kawahara et al, and SGS-Thomson in regard to the distinguishing subject matter recited in the claims discussed above.

Accordingly, it is respectfully submitted that the rejections based on Kawahara et al. and SGS-Thomson and Kawahara et al., SGS-Thomson and Kobayashi et al. are clearly in error and that the teachings and suggestions of those reference do not, in fact, answer the explicit recitations of the claims, particularly in regard to a changing point detection means *in addition to* a power-on reset circuit and initiating reset in response to *either* the changing point detection means *or* the power-on reset circuit. Therefore, reconsideration and withdrawal thereof is respectfully requested.

In this regard, it is again respectfully submitted that entry of the above-requested amendments is well-justified. It is clear that no new issue can be raised in the addition of language to one claim which was already present in another claim as finally rejected. Further, it is respectfully submitted that the finality of the present office action is premature since no action should be made final which does not include a *prima facie* demonstration of the propriety of the grounds of rejection contained therein, particularly when the rejections are repeated in spite of the same failure to make a *prima facie* demonstration of the propriety of the rejections in the previous action as pointed out in the response thereto and without comment by the Examiner on that issue in the present action. Therefore, it is respectfully submitted that the finality of the present action should be withdrawn and

the above-requested amendments entered as a matter of right. In any case, entry of the above-requested amendments are also well-justified as clear placing the application in condition for allowance or, in the alternative, as placing the application in better form for appeal by materially reducing and simplifying issues.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

A petition has been made, above, for a one-month extension of time for response. If any further extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,

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